# 9 ROM, EPROM, AND EEPROM TECHNOLOGY

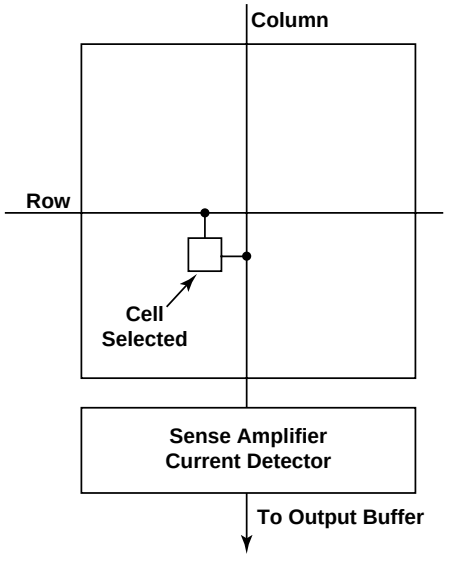
## OVERVIEW

Read only memory devices are a special case of memory where, in normal system operation, the memory is read but not changed. Read only memories are non-volatile, that is, stored information is retained when the power is removed. The main read only memory devices are listed below:

ROM (Mask Programmable ROM—also called “MROMs”)
EPROM (UV Erasable Programmable ROM)
OTP (One Time Programmable EPROM)
EEPROM (Electrically Erasable and Programmable ROM)
Flash Memory - This device is covered in Section 10.

## HOW THE DEVICE WORKS

The read only memory cell usually consists of a single transistor (ROM and EPROM cells consist of one transistor, EEPROM cells consist of one, one-and-a-half, or two transistors). The threshold voltage of the transistor determines whether it is a “1” or “0.” During the read cycle, a voltage is placed on the gate of the cell. Depending on the programmed threshold voltage, the transistor will or will not drive a current. The sense amplifier will transform this current, or lack of current, into a “1” or “0.” Figure 9-1 shows the basic principle of how a Read Only Memory works.




*Source: ICE, "Memory 1997"* 19956

**Figure 9-1. Read Only Memory Schematic**

## MASK PROGRAMMABLE ROMs

Mask programmable read-only memories (ROMs) are the least expensive type of solid state memory. They are primarily used for storing video game software and fixed data for electronic equipment, such as fonts for laser printers, dictionary data in word processors, and sound data in electronic musical instruments.

ROM programming is performed during IC fabrication. Several process methods can be used to program a ROM. These include

- Metal contact to connect a transistor to the bit line.
- Channel implant to create either an enhancement-mode transistor or a depletion-mode transistor.
- Thin or thick gate oxide, which creates either a standard transistor or a high threshold transistor, respectively.

The choice of these is a trade-off between process complexity, chip size, and manufacturing cycle time. A ROM programmed at the metal contact level will have the shortest manufacturing cycle time, as metallization is one of the last process steps. However, the size of the cell will be larger.

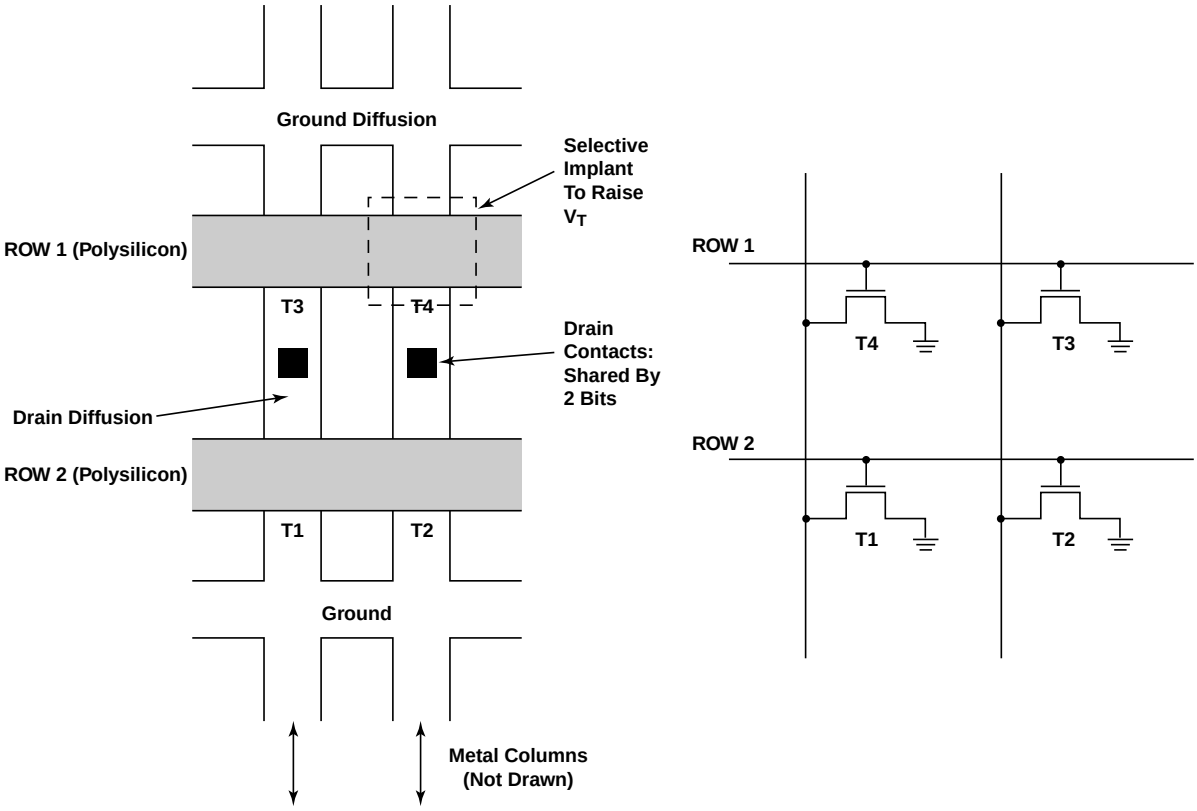
Figure 9-2 shows a ROM array programmed by channel implant. The transistor cell will have either a normal threshold (enhancement-mode device) or a very high threshold (higher than $V_{CC}$ to assure the transistor will always be off). The cell array architecture is NOR. The different types of ROM architectures (NOR, NAND, etc.) are detailed in the flash memory section (Section 10) as they use the same principle.

Figure 9-3 shows an array of storage cells (NAND architecture). This array consists of single transistors noted as devices 1 through 8 and 11 through 18 that is programmed with either a normal threshold (enhancement-mode device) or a negative threshold (depletion-mode device).

### ROM Cell Size and Die Size

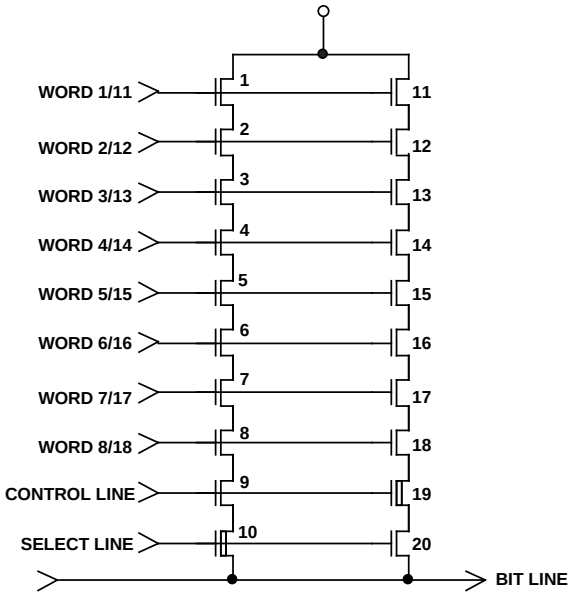
The cell size for the ROM is potentially the smallest of any type of memory device, as it is a single transistor. A typical 8Mbit ROM would have a cell size of about 4.5µm$^2$ for a 0.7µm feature size process, and a chip area of about 76mm$^2$. An announced 64Mbit ROM, manufactured with a 0.6µm feature size, has a 1.23µm$^2$ cell on a 200mm$^2$ die.

The ROM process is the simplest of all memory processes, usually requiring only one layer of polysilicon and one layer of metal. There are no special film deposition or etch requirements, so yields are the highest among all the equivalent-density memory chips.




*Source: ICE, "Memory 1997"* 20845

**Figure 9-2. ROM Programmed by Channel Implant**




*Source: ICE, "Memory 1997"* 19050

**Figure 9-3. Memory Cell Schematic**